Bulletin of Electrochemistry 2 (2) Mar.-Apr. 1986 pp. 181-183

FABRICATION OF Cu_2S-CdS SOLAR CELL USING SCREEN PRINTED CdS LAYERS

M JAYACHANDRAN, (MRS) MARY JULIANA CHOCKALINGAM, K NAGARAJA RAO, I RADHAKRISHNA and N RANGARAJAN
Central Electrochemical Research Institute, Karaikudi - 623 006

ABSTRACT

Cadmium sulphide layers have been prepared on various substrates by the screen printing and sintering technique on conducting and non-conducting substrates. These layers have been annealed in vacuum at 350° C for obtaining enhanced conductivity. Cuprous sulphide layers have been obtained on these layers by the Clevite process. Post heat-treatment has been carried out in air to form the required p-n heterojunctions. Solar cells have been fabricated and the output characteristics have been studied.

Key words: Cu_2S-CdS solar cell, screen printing, sintering

INTRODUCTION

CdS layers have been obtained by various methods such as vacuum evaporation [1], sputtering [2] (reactive sputtering of Cd in H_2S), spray pyrolysis [3,4], screen printing and sintering [5], vapour deposition and electrodeposition [6] to yield solar cells with efficiencies close to that of single crystal values.

Although vacuum evaporation of CdS followed by the conventional Clevite wet process has been the popular method for fabrication of solar cells, methods like spray pyrolysis and sintering seem to have a promising future, because of their low cost of production/unit power.

Hence, in this paper the screen printing technique, sintering of CdS and its effect on different substrates are discussed. CdS layers sintered on ceramic substrates were used for making layer type cells by Clevite process. The output of the cells are reported and compared.

EXPERIMENTAL

Sintered CdS layers made by screen printing technique

Photograde CdS powder was prepared by the thiourea method developed in this laboratory [7]. This powder was sensitized with cadmium chloride, evaporated to dryness and ground well so as to pass through 400 mesh sieve. A uniform coating was given on stainless steel, molybdenum, and ceramic substrates by silk screen technique. These layers were dried at 120° C in air and sintered between 500-600° C under controlled atmosphere in Gallenkamp Furnace with proportional control.

The CdS layers prepared with cadmium chloride alone as the flux material yielded high resistance layers of the order of 100 k.ohms. To bring down the resistance, $CdSO_4$ was added along with 10% cadmium chloride. Four samples with various concentrations of $CdSO_4$ (1-4 %) were prepared and cells were fabricated from each batch. The CdS layers thus obtained and vacuum annealed at 350° C at 10^{-5} torr for 45 minutes [8] gave rise to a layer with dark resistivity of 2.5 ohm-cm.

Substrate effect on CdS layer

When attempts were made to get thin CdS layers on metallic substrates by sintering technique, the substrate material and the surface preparation conditions were found influencing the characteristics of the CdS layers. Vacuum evaporated layers on different conducting substrates such as zinc-coated copper, zinc, molybdenum, aluminium-coated copper, iron-nickel and cadmium stannate and electroformed copper foil was studied extensively [9]. However, no reports are found on the substrate effect of the screen printed and sintered CdS layers.

Substrate treatment

CdS films were formed on molybdenum sheet etched in 1:1 HNO_3; stainless steel sheet etched in 25 % ferric chloride and 5 % HCl and ceramic substrates. Uniform and adherent coatings could be obtained on etched stainless steel substrates. Preheated Mo and stainless steel substrates gave better adherence perhaps due to the formation of low resistance mono-molecular oxide layer.

Etching of CdS layer

Etching of the CdS layer is a necessary step as it opens up the crystallites for the topotaxial growth of Cu_2S and leads to maximum coverage of the CdS layer. Attempts to etch the sintered CdS layer on ceramic substrate with 1 : 1 HCl gave good output. Shorting of the latter was observed in the case of metallic substrates. Hence sintering on metallic substrates not only warranted thick layers unlike in the case of ceramic substrates but also different sintering conditions.

Morphology of CdS layer on different substrates

Figure 1 (a, b, c) shows the SEM pictures of CdS sintered layers on Mo, stainless steel and ceramic substrate respectively. The degree of conglomeration of grains decreases in the order ceramic, Mo and stainless steel. Less number of pits are seen in the CdS layer on the ceramic substrate. Mo substrate has greater number of pits, but are uniformly distributed. When double coating is given and compacted, it leads to uniform layer. On stainless steel substrate, larger and deeper pits are seen which lead to microcracks and shorting when Cu_2S is formed over the layer. The pit formation can be attributed to the differential thermal expansion between the metal substrate and CdS layer.

At the higher magnification, the spherical crystalline structure of the CdS layer is well brought out in figure 2 (a,b). The grain size lies in the range 1.5 μm to 3.5 μm. The crystalline structure is better in Mo (2 a) than in the case of stainless steel (2 b) or ceramic substrate.

Heterojunction formation

Various processes are available in the literature [10] for the formation of Cu_2S film on CdS layer such as: the Clevite process, solid state reaction (dry process), electrodeposition, vacuum deposition and spraying methods.

The vacuum annealed CdS layers were etched in 1 : 1 hydrochloric acid for two seconds at room temperature. Then washed in triple distilled water followed by acetone and dried. A bath containing 1% cuprous chloride, 5% sodium chloride and traces of [illegible] was maintained at 90° C.

The CdS layer was dipped for 10 seconds and Cu_2S layer was formed. It was washed in triple distilled water to remove the soluble $CdCl_2$ and then in acetone and dried at 110° C. As such no rectification was observed and a post heat-treatment was given to form the junction.

In this work, the cells were annealed at 200° C in air for different timings. The optimum time for maximum V_{oc} and I_{sc} was found to be 14 minutes.

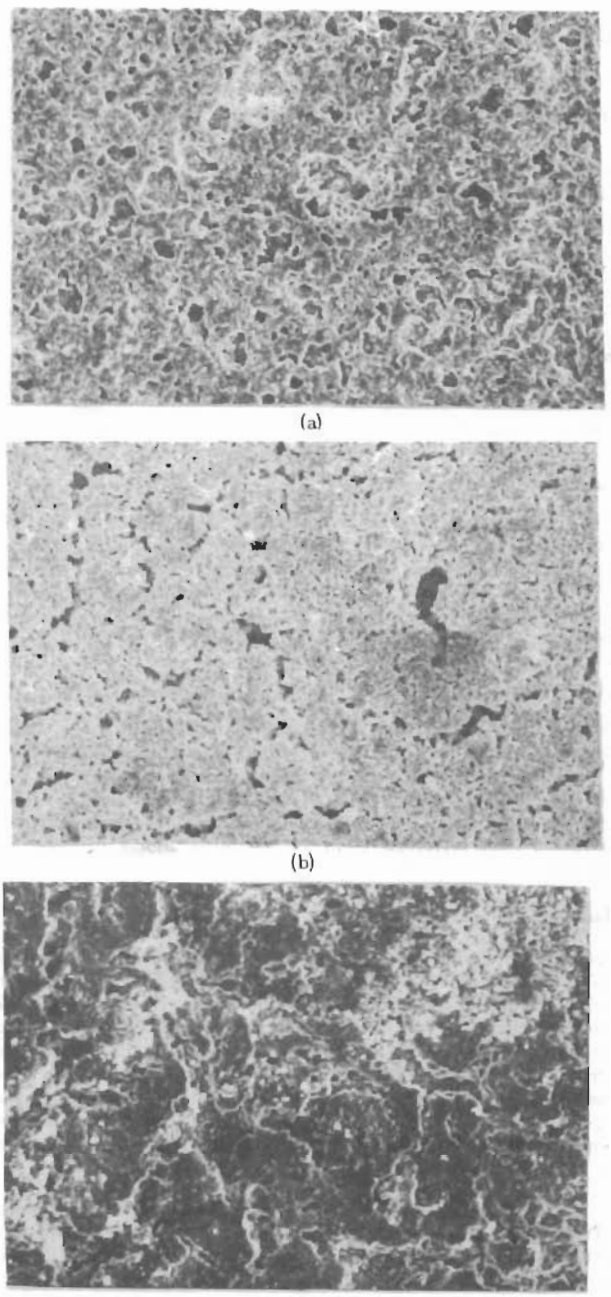

Fig. 1: Sintered CdS on different substrates (X270): (a) Mo (b) Stainless steel (c) Ceramic

Solar cell fabrication

In order to study the behaviour and contribution of the prepared low-resistance CdS layer with Cu_2S layer on the same, layer-type solar cells were fabricated as shown in figure 3. It consisted of a sintered polycrystalline CdS layer of about 30 μm on a ceramic substrate. An indium coating covering about 10% of the CdS surface was formed and then annealed at about 360° C at a pressure of 10^{-5} torr for one hour. The Cu_2S was formed over the CdS layer leaving some space between In contact and the Cu_2S layer. Silver paste was applied to the Cu_2S layer. Leads were connected to the indium and silver contacts to serve as negative and positive terminals of the cells. Polystyrene lacquering was done over this and the whole system was encapsulated in an acrylic cup. It was then hermetically sealed with epoxy resin to prevent the entry of atmospheric O_2 or water vapour into the system.

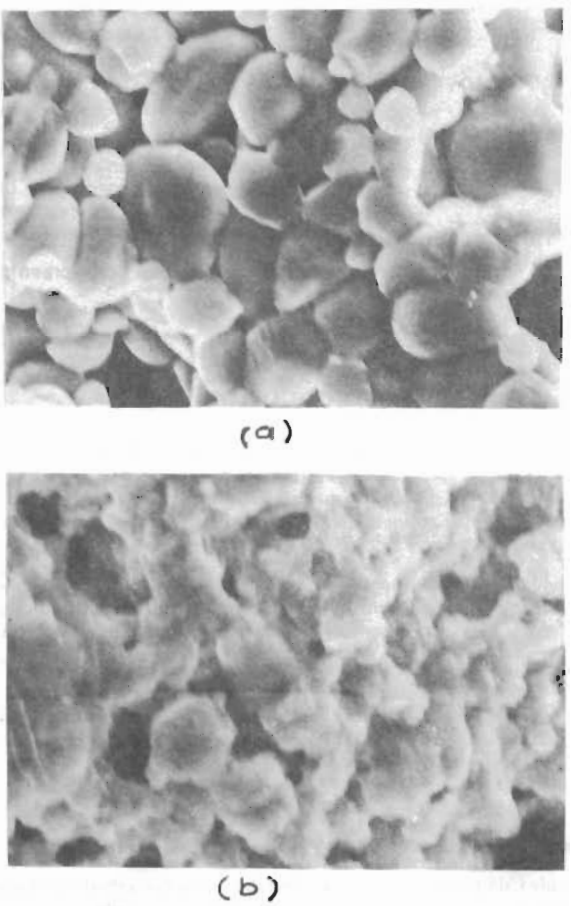

Fig. 2: Sintered CdS (X2700) on (a) Mo and (b) Stainless steel

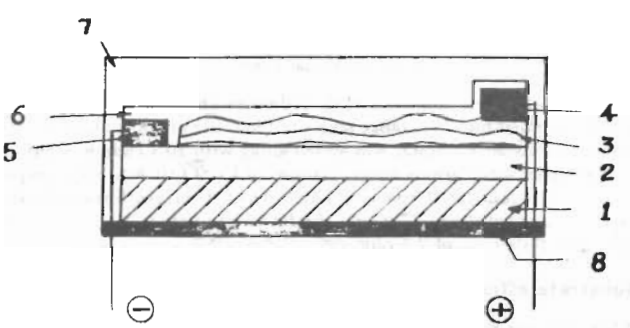

Fig. 3: Schematic diagram of the ceramic substrate Cu_2S/CdS solar cells: 1) Ceramic substrate 2) CdS 3) Cu_2S 4) Silver contact 5) Indium contact 6) Lacquering 7) Encapsulant 8) Epoxy seal

RESULTS AND DISCUSSIONS

The variation of photosensitivity with time is well brought out in the figure 4. Although various percentages of addition of $CdSO_4$ to the sensitized powder were tried, the addition of 2% and 3% of $CdSO_4$ gave R_D/R_L values in the useful range (since the CdS required for photovoltaic work should not only have a low resistance but R_D/R_L value tending to 1). As is shown in the figure the sensitivity is maximum for 40 minutes sintering time for 2% $CdSO_4$ as well as 3% $CdSO_4$. During sintering, the cadmium chloride melts at 585°C and CdS dissolves in the molten cadmium chloride to initiate recrystallisation. Beyond optimized time and temperature, $CdCl_2$ volatilizes away.

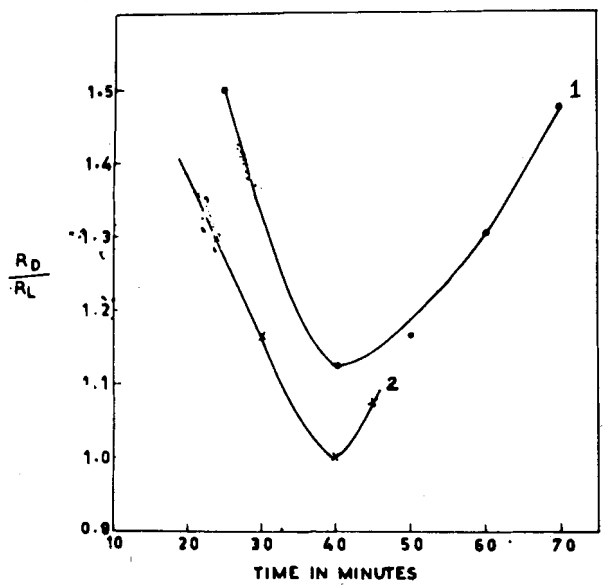

Fig. 4: Effect of sintering on CdS layer resistance:

1) 2% $CdSO_4$ and 2) 3% $CdSO_4$

Effect of cadmium sulphate on the resistance of CdS

The addition of $CdSO_4$ brings about an increase in Cd^{++}/S^{--} ratio as revealed by the reactions

$$CdS + CdSO_4 \rightarrow 2Cd^{++} + 2SO_2\uparrow$$

$$(1-x)\,CdS + xCd^{++} \rightarrow CdS_{1-x}$$

CdS reacts with $CdSO_4$ to form more Cd^{++} ions and the evolution of SO_2 from the lattice creates more sulphur vacancy. As a result, Cd^{++}/S^{--} ratio increases which is reponsible for the lower resistance of the layer. Above 3%, $CdSO_4$ remains as such in the lattice and this being an insulator does increase the resistance. Below 3% $CdSO_4$ sufficient Cd^{++}/S^{--} ratio is not built for want of $CdSO_4$. Hence the high resistance.

Role of cadmium chloride

Figure 4 shows a decrease in the values of R_d/R_L with time up to 40 minutes and then a rise, which is due to the fact that more and more chloride ions are getting incorporated into the lattice giving rise to more donor levels. Above the sintering time of 40 minutes, more and more of chloride ions begin to get out of the lattice gradually thereby decreasing the donor concentration.

Even though Mo substrate is the best choice with spherical grain structure for maximum efficiency [11] followed by stainless steel substrate, the cost, short circuiting and peeling-off of the layers after Cu_2S formation are the unfavourable factors, when low cost cells with reasonable conversion efficiency are aimed.

The V_{oc} and I_{sc} of the final cell with varied parameters are given in Table I.

Table I: Properties of Cu_2S–CdS Solar cells

Cell No.	Deposition time (sec)	Sheet resistance of $Cu_{2-x}S$ (ohms per sq.)	Time of heat treatment (minutes)	V_{oc} (mV)	I_{sc} (mA/cm^2)
1	10	120	5	397	0.60
37	5	140	10	425	1.17
61	10	160	12	240	2.50
62	10	200	14	370	6.00
64	10	140	15	340	1.78

Maximum I_{sc} was obtained for the cell No. 62 whose Cu_2S sheet resistance is maximum. When the post heat-treatment time was increased from 5 to 14 minutes, the Cu_2S sheet resistance also increased from 120 ohms to 200 ohms/square. This may be due to the diffusion of cadmium ions into the Cu_2S lattice. The Cu_2S being p-type, cadmium ion entering the lattice as donors brings about an increase in resistance [2]. However, the resistance decreases when post heat treatment time exceeds 14 minutes. This may perhaps be attributed to the number of copper ions entering the CdS lattice exceeding the number of cadmium ions entering the Cu_2S lattice. Thus a post heat treatment of 14 minutes tends to form the chalcocite phase of the Cu_2S layer which absorbs most of the incident solar radiation [13] for current generation. Also a recent work [14] on the physicochemical properties confirms the observation that the resistivity is more when the Cu content in the Cu_xS layer increases and is maximum for Cu_2S.

CONCLUSION

The addition of 3% $CdSO_4$ is necessary to obtain low-resistance, sintered CdS layers and thereby increasing the cell output.

Further investigations are being continued to increase the sheet resistance of the cuprous sulphide layer and optimize the conditions for chalcocite (near Cu_2S) formation for getting maximum output.

Acknowledgement: The authors thank Dr V K Venkatesan, Head, Electrochemical Materials Science Division for helpful discussions. The authors also thank Sri R Mahalingam for helping them in getting some of the layers vacuum annealed.

REFERENCES

1. L C Burton, *Solar Cells*, **1** (1980) 159
2. W Mueller, H Freg, K Radler and K H Schuller, *Thin Solid Films*, **59** (1979) 327
3. R R Chamberlin and J S Skarman, *J Electrochem Soc*, **113** (1966) 86
4. L Escosura, E Garcia-Camarero, F Arjona and F Rueda, *Solar Cells*, **11** (1948) 211
5. H Matsumato, N Nakayama and S Ikegami, *Jpn J Appl Phys*, **19** (1980) 129
6. J F McCann and M Skyllas Kazacas, *J Electroanal Chem*, **119** (1981) 409
7. C V Suryanarayana, N Rangarajan, K Nagaraja Rao and Mary Juliana Chockalingam, Indian Patent No. 115347 (1968)
8. Mary Juliana Chockalingam, R Mahalingam, K Nagaraja Rao, I Radhakrishna, N Rangarajan and C V Suryanarayana, *Bull Electrochem*, **1** (1985) 70
9. L C Burten, International Workshop on "CdS solar cells and other heterojunctions", April 30-May 2 (1975) p 305
10. M Savelli and J Bougnot, *Solar Energy Conversion* Ed. B O Seraphin, Springer Verlag, N.Y. (1979) 213
11. H Saha and S Banerjee, *Solar Cells*, **7** (1982) 233
12. F J Bryant, A K Hani, S Salkalachen and C G Scott, *J Phys D : Appl Phys*, **16** (1983) 1755
13. W Palz and J Bessen, *Photovoltaic Specialists Conf*, May 2-4 (1975) p 91
14. H Rickert, H D Wienhafer, T E Schmidt, R Wagner, *Proc Fourth E C Photovoltaic Solar Energy Conference*, (1982) 827